REMARKS/ARGUMENTS

Claims 1-17 are pending in the application. Claims 1-17 are rejected.

Claim Rejections under 35 U.S.C. § 102

Claims 1-15 are rejected under 35 U.S.C. §102(b) as being anticipated by Castle et al., U.S. Patent No. 5,813,034 (hereinafter "Castle"). Castle discloses a multi-level distributed data processing system comprised of: a system bus having a main memory coupled thereto; multiple high level cache memories, each of which has a first port coupled to the system bus and a second port coupled to a respective processor bus; and, each processor bus is coupled to multiple digital computers through respective low level cache memories. (see *Abstract, Brief Summary of the Invention* col. 2, ll.32-39, *Claim 1* col. 17, ll. 41-48). Castle discloses a system of high-level and low-level cache memories, each low-level cache storing data for one processor, and each high-level cache storing data for each data processing cluster. Applicants respectfully submit that Castle does not suggest or disclose a method and apparatus for distributed caches in a single cache-coherent CPU or I/O device serving multiple CPU port components or I/O components, but rather, a system with *multi-level cache memory* in order to maintain coherency across a *multi-processor distributed data processing system.* (see Fig. 1)

As per claim 1, the Examiner compares Fig. 16 of Castle to the cache-coherent device as claimed by Applicants. Applicants respectfully submit that Fig. 16 is not representative of the method and apparatus of distributed caches as disclosed by Applicants. The Examiner goes even further to compare tag memory 91 and tag memory 96 of Fig. 16 to the sub-unit caches as disclosed by Applicants. Castle describes modules 91 and 96 as "tag-memory, which stores the same compare addresses and tag bits (E, S, M and I) for each stored address." (see Table 1,

modules 91 and 96, col. 9) These tag-memory modules are not used for storing data as described by Applicants for distributed read/write caches 110, 115 and 120. In Applicants' disclosure, in one embodiment, "coherency engine 105 contains a directory, indexing all the data within distributed caches 110, 115 and 120." (see Application, p. 5, ll. 5-7)

Furthermore, Fig. 16 of Castle makes no mention of a distributed cache system, only a *single* data memory unit, described as module 92. (see Table 1, col. 9) Applicants respectfully submit that Examiner's arguments regarding the data processing system of Fig. 16 in Castle does *not* describe the method and apparatus for the utilization of distributed caches as disclosed by Applicants. Outside the confines of the Examiner's arguments, Applicants submit that Castle generally describes a multi-leveled memory system for modifying data words in a data processing system configured for multiple processors, not a device and method for utilizing distributed caches for multiple CPU or I/O components.

Therefore, Applicants respectfully submit that claim 1 is allowable. As per independent claims 6 and 9, the foregoing arguments may also be applied. Sub-unit caches in a method and apparatus for the utilization of distributed caches are not described by any of Figs. 9-17 of Castle (in reference to Examiner's suggestion concerning modules 91 and 96). In addition, Applicants respectfully submit that claims 2-5, 7, 8, 10-15 are allowable as depending from an allowable base claims 1, 6 and 9.

Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 1-15 under 35 U.S.C. § 102(b) is respectfully requested.

Claim Rejections under 35 U.S.C. § 103

Claims 16-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Castle et al., U.S. Patent No. 5,813,034 in view of Witt et al., U.S. Patent No. 6,202,139 (hereinafter "Witt").

Applicants respectfully submit that claims 16 and 17 are allowable as depending from an allowable base claim 9 given the arguments above.

With respect to Examiner's argument, Witt discloses a pipelined data cache with multiple ports. The invention is described as a computer system including a processor having a cache which includes multiple ports. The cache is pipelined and operates at a clock frequency higher than that employed by the remainder of the microprocessor including the cache for multiple accesses per clock cycle. (see *Abstract, Summary of the Invention*, col. 2, ll.31-36)

As per claim 16, Witt discloses that multiple accesses are advantageously gained by operating the cache at a higher frequency, with the resulting accessing being pipelined instead of applied to separate banks. However, Applicants disclose that, in one embodiment of the invention, write transactions are pipelined by forwarding the write transaction to the front-side bus or by holding up the cache line state. (see Application, pg. 10, ll. 7-17) Therefore, Applicants respectfully submit that claim 16 is allowable. In addition, Applicants respectfully submit that claim 17 is allowable as depending from an allowable base claims 16.

In addition and in the alternative, Applicants respectfully submit that there is no suggestion or motivation to combine Castle and Witt beyond the impermissible use of hindsight. Applicants submit that a *prima facie* case of obviousness has not been made. The MPEP requires that the references must suggest making the combinations. MPEP §2141.01 (citing

Hodosh v. Block Drug Co., Inc.); §706.02(j) (the initial burden is on the examiner to provide a convincing line of reasoning with explicit or implicit suggestions to combine references).

Merely stating that it would have been obvious for a person of ordinary skill in the art to combine references, without pointing to a specific hint or suggestion to combine, has been rejected by the Federal Circuit, as an invalid basis of rejection under 35 U.S.C. §103. *In re Lee*, 277 F.3d 1338, 1343 (Fed. Cir. 2002)(the court held that rejecting a conclusory statement that it would have been obvious to combine the references without evidence of a teaching, motivation, or suggestion to select and combine the references, citing numerous case); *In re Dembiczak*, 175 F.3d 994,999 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.")

The Applicants therefore respectfully request Examiner to provide specific evidence of the teaching to combine Castle and Witt references or withdraw the rejection as improper.

Based on the foregoing arguments and amendments, Applicants respectfully submit that 16 and 17 are allowable.

.Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 16-17 under 35 U.S.C. § 103(a) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600.**

Respectfully submitted,

KENYON & KENYON

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By: _____

Edward S. Quon
(Reg. No. 52,144)
Attorneys for Intel Corporation

KENYON & KENYON
333 West San Carlos St., Suite 600
San Jose, CA 95110

Telephone: (408) 975-7500
Facsimile: (408) 975-7501